

Claims

[c1] What is claimed is:

1. A digital phase frequency discriminator (DPFD) comprising:

a first SR latch for generating a first output signal when being set to a predetermined state, the first SR latch comprising a first input end for receiving a first input signal;

a second SR latch for generating a second output signal when being set to the predetermined state, the second SR latch comprising a first input end for receiving a second input signal;

a predetermined state detection circuit electrically connected to the first and the second SR latches for detecting the first and the second output signals and for outputting an RCM signal;

a first predetermined state control circuit electrically connected to the predetermined state detection circuit and the first SR latch for setting the first SR latch to the predetermined state according to the RCM signal, the first predetermined state control circuit comprising a first input end for receiving the first input signal, and a second input end for receiving the RCM signal; and

a second predetermined state control circuit electrically connected to the predetermined state detection circuit and the second SR latch for setting the second SR latch to the predetermined state according to the RCM signal, the second predetermined state control circuit comprising a first input end for receiving the second input signal, and a second input end for receiving the RCM signal.

[c2] 2. The DPFD of claim 1 further comprising a first delay component electrically connected between the first input end of the first predetermined state control circuit and the first input end of the first SR latch.

[c3] 3. The DPFD of claim 2 further comprising a second delay component electrically connected between the first input end of the second predetermined state control circuit and the first input end of the second SR latch.

[c4] 4. The DPFD of claim 1, wherein the predetermined state detection circuit comprises a NAND gate.

[c5] 5. The DPFD of claim 4, wherein the first SR latch comprises a Q output signal end, the second SR latch comprises a Q output signal end, and the NAND gate comprises two input ends electrically connected to the two Q output signal ends respectively.

[c6] 6. The DPFD of claim 1, wherein the predetermined state

detection circuit comprises an OR gate.

- [c7] 7. The DPFD of claim 6, wherein the first SR latch comprises a



output signal end, the second SR latch comprises a



output signal end, and the OR gate comprises two input ends electrically connected to the two



output signal ends respectively.

- [c8] 8. The DPFD of claim 1, wherein both the first and the second SR latches comprise a pair of cross-coupled NOR gates.

- [c9] 9. The DPFD of claim 1, wherein both the first and the second SR latches comprise a pair of cross-coupled NAND gates.

- [c10] 10. The DPFD of claim 1, wherein both the first and the second predetermined state control circuits comprise a pair of cross-coupled NAND gates.

[c11] 11. The DPF_D of claim 1, wherein both the first and the second predetermined state control circuits comprise a pair of cross-coupled NOR gates.